



Typical Applications

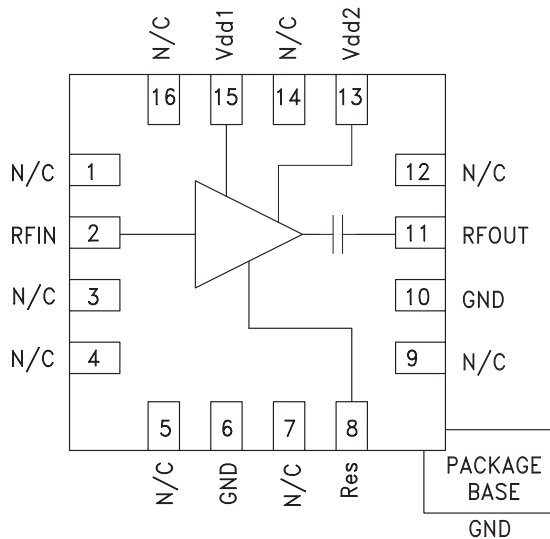
The HMC618LP3E is ideal for:

- Cellular/3G and LTE/WiMAX/4G
- BTS & Infrastructure
- Repeaters and Femto Cells
- Public Safety Radios

Features

- Noise Figure: 0.75 dB
- Gain: 19 dB
- OIP3: 36 dBm
- Single Supply: +3V to +5V
- 50 Ohm Matched Input/Output
- 16 Lead 3x3mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC618LP3E is a GaAs PHEMT MMIC Low Noise Amplifier that is ideal for Cellular/3G and LTE/WiMAX/4G basestation front-end receivers operating between 1.7 - 2.2 GHz. The amplifier has been optimized to provide 0.75 dB noise figure, 19 dB gain and +36 dBm output IP3 from a single supply of +5V. Input and output return losses are excellent and the LNA requires minimal external matching and bias decoupling components. The HMC618LP3E shares the same package and pinout with the HMC617LP3E 0.55 - 1.2 GHz LNA. The HMC618LP3E can be biased with +3V to +5V and features an externally adjustable supply current which allows the designer to tailor the linearity performance of the LNA for each application. The HMC618LP3E is an ideal replacement for the HMC375LP3E.

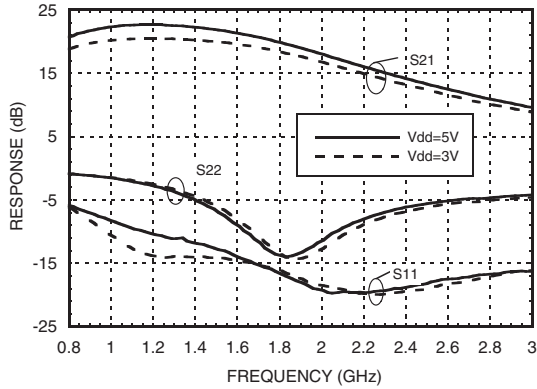
Electrical Specifications, $T_A = +25^\circ C$, $R_{bias} = 10K$

Parameter	Vdd = 3 Vdc						Vdd = 5 Vdc						Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	1700 - 2000			2000 - 2200			1700 - 2000			2000 - 2200			MHz
Gain	15	18		12.5	15.8		16	19		13.5	17		dB
Gain Variation Over Temperature		0.009			0.009			0.008			0.008		dB/°C
Noise Figure		0.90	1.2		0.9	1.2		0.75	1.1		0.85	1.15	dB
Input Return Loss		17			19			18			19.5		dB
Output Return Loss		13			11			12.5			9.5		dB
Output Power for 1 dB Compression (P1dB)	12	15		13.5	15		16.5	20		18	20		dBm
Saturated Output Power (Psat)		16			16			20.5			21		dBm
Output Third Order Intercept (IP3)		28			28			35			36		dBm
Supply Current (Idd)		47	65		47	65		117	155		117	155	mA

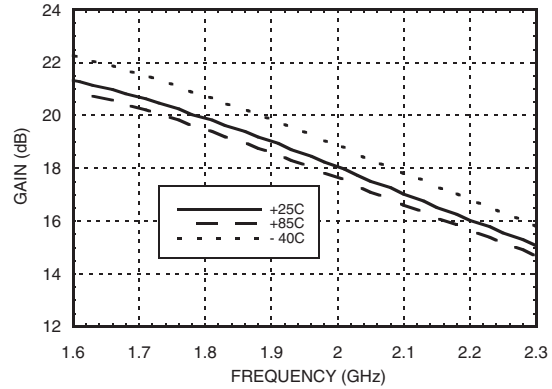
* Rbias resistor sets current, see application circuit herein



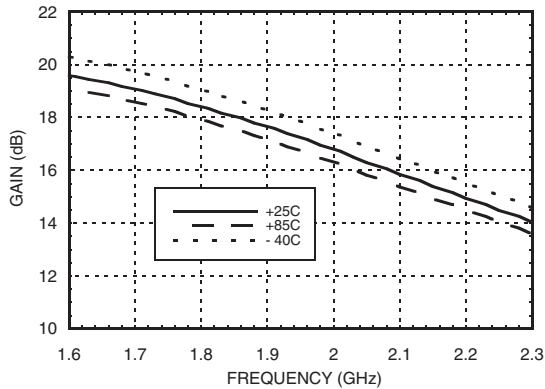
Broadband Gain & Return Loss^{[1] [2]}



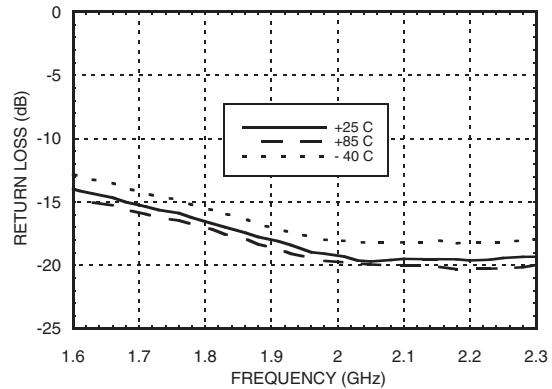
Gain vs. Temperature^[1]



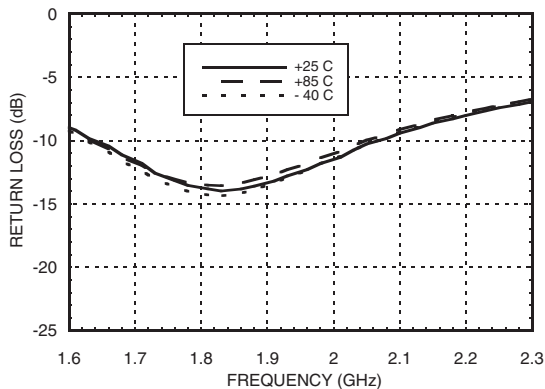
Gain vs. Temperature^[2]



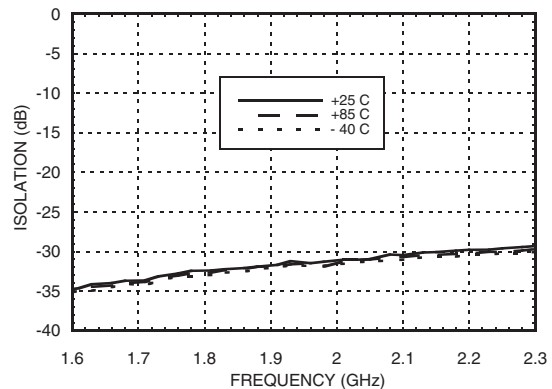
Input Return Loss vs. Temperature^[1]



Output Return Loss vs. Temperature^[1]

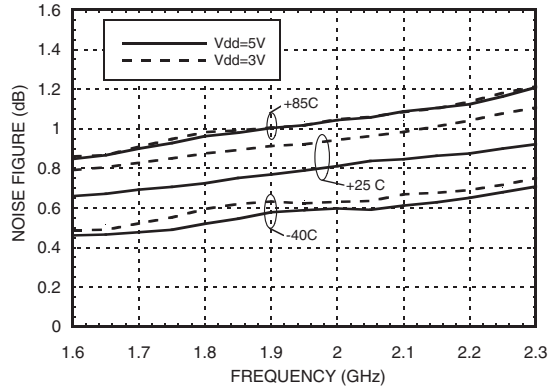


Reverse Isolation vs. Temperature^[1]

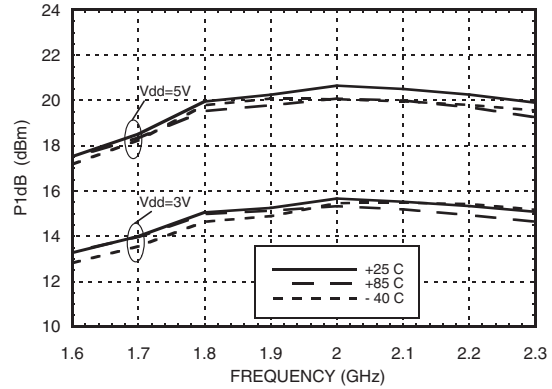


[1] Vdd = 5V, Rbias = 10K [2] Vdd = 3V, Rbias = 10K

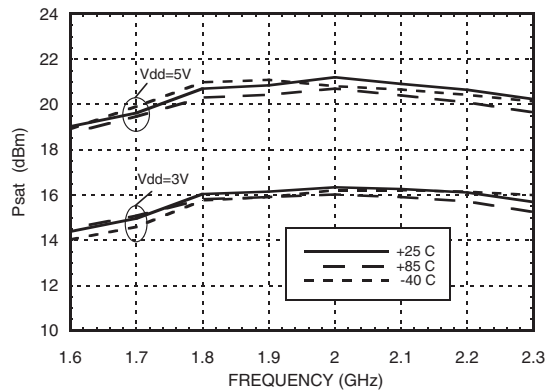
Noise Figure vs Temperature ^{[1] [2] [4]}



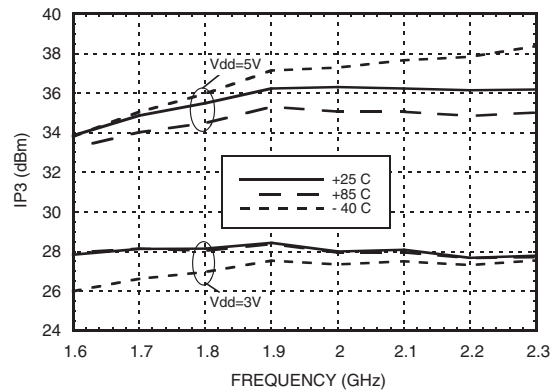
Output P1dB vs. Temperature ^{[1] [2]}



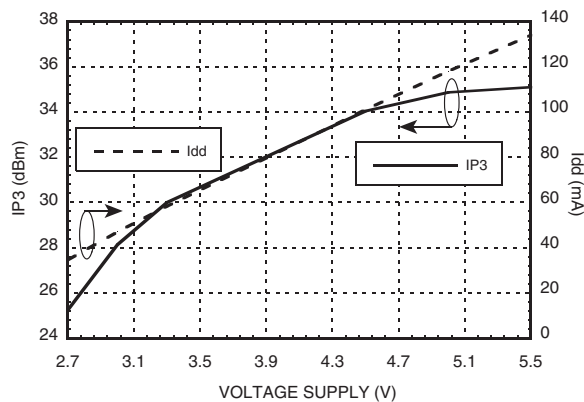
Psat vs. Temperature ^{[1] [2]}



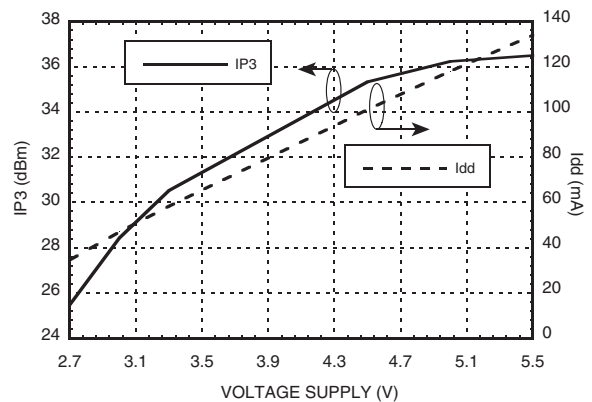
Output IP3 vs. Temperature ^{[1] [2]}



Output IP3 and I_{dd} vs. Supply Voltage @ 1750 MHz ^[3]



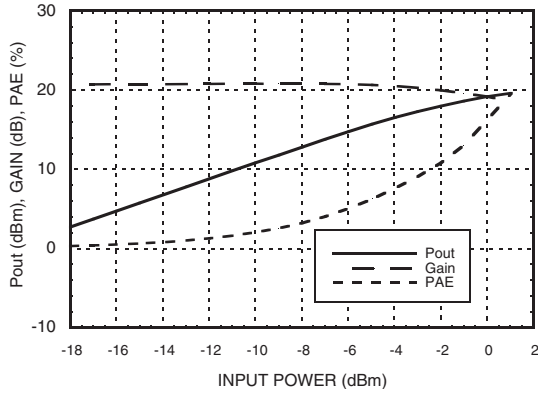
Output IP3 and I_{dd} vs. Supply Voltage @ 2100 MHz ^[3]



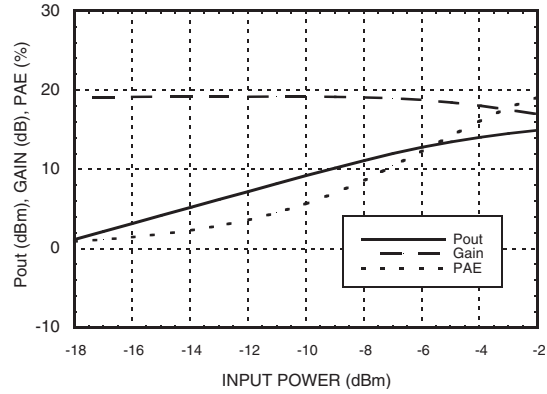
[1] V_{dd} = 5V, R_{bias} = 10K [2] V_{dd} = 3V, R_{bias} = 10K

[3] R_{bias} = 10K [4] Measurement reference plane shown on evaluation PCB drawing.

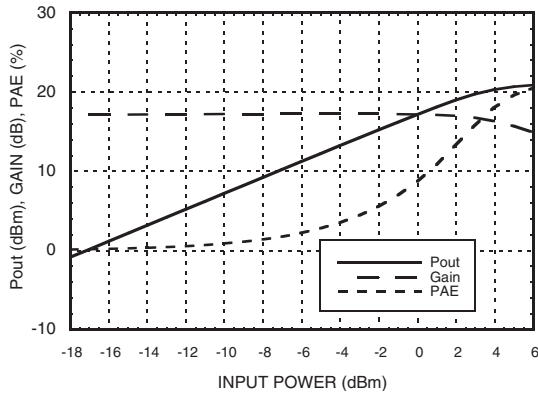
Power Compression @ 1750 MHz [1]



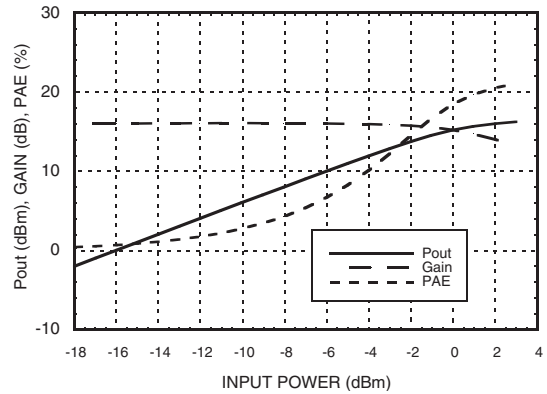
Power Compression @ 1750 MHz [2]



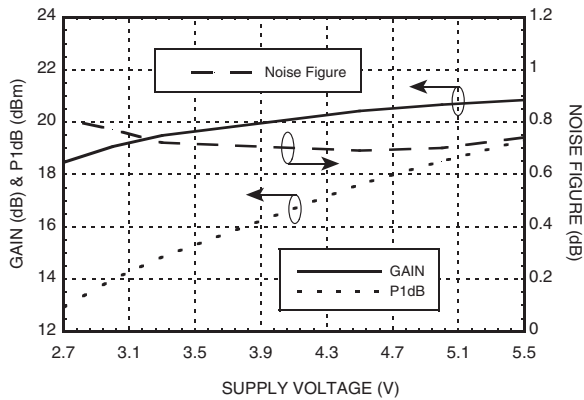
Power Compression @ 2100 MHz [1]



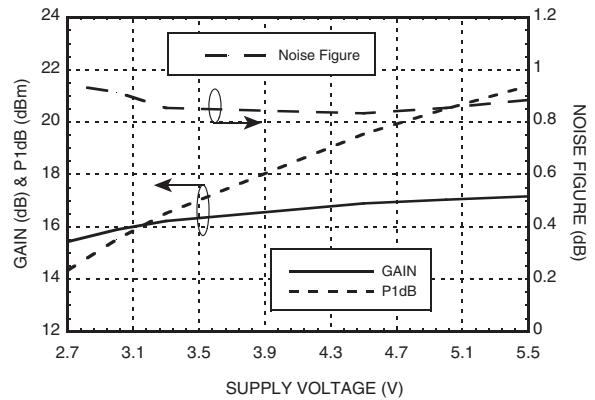
Power Compression @ 2100 MHz [2]



Gain, Power & Noise Figure vs. Supply Voltage @ 1750 MHz [3]

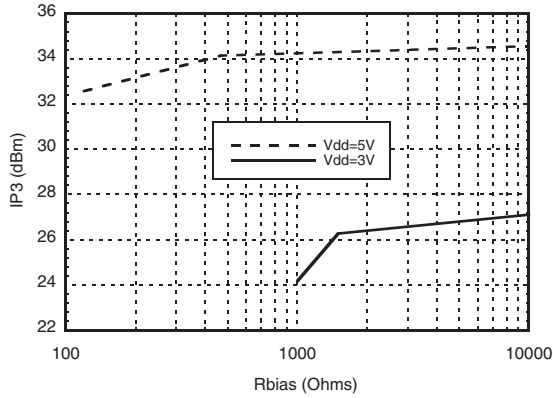


Gain, Power & Noise Figure vs. Supply Voltage @ 2100 MHz [3]

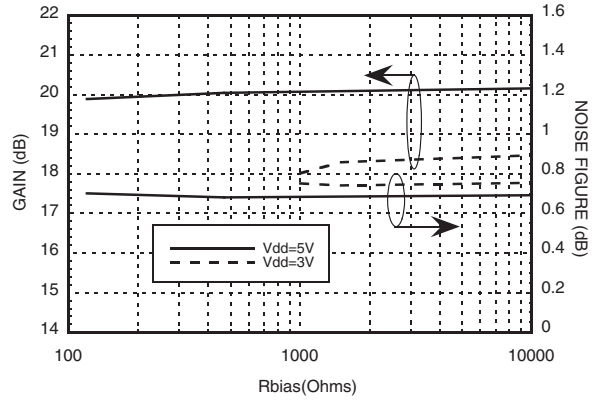


[1] Vdd = 5V, Rbias = 10K [2] Vdd = 3V, Rbias = 10K [3] Rbias = 10K

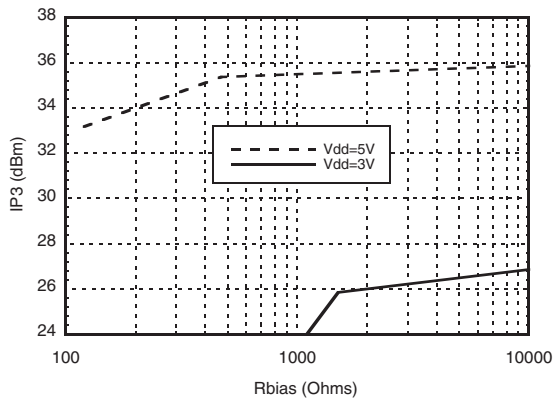
Output IP3 vs. Rbias @ 1750 MHz



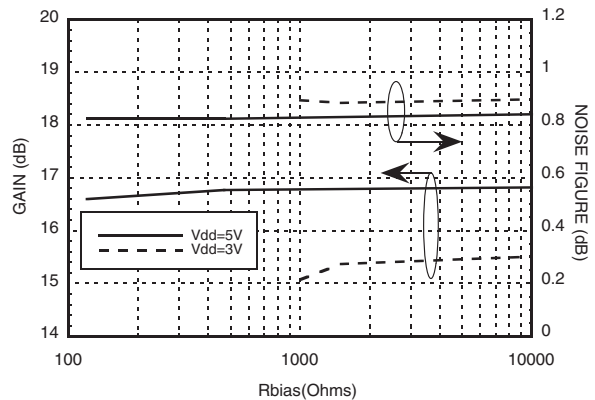
Gain, Noise Figure & Rbias @ 1750 MHz



Output IP3 vs. Rbias @ 2100 MHz



Gain, Noise Figure & Rbias @ 2100 MHz



Absolute Bias Resistor

Range & Recommended Bias Resistor Values for Idd

Vdd1 = Vdd2 (V)	Rbias			Idd1 + Idd2 (mA)
	Min (Ohms)	Max (Ohms)	R1 (Ohms)	
3V	1K [1]	Open Circuit	1k	28
			1.5k	34
			10k	47
5V	0	Open Circuit	120	71
			470	89
			10k	117

[1] With Vdd= 3V and Rbias < 1K Ohm may result in the part becoming conditionally stable which is not recommended.



Absolute Maximum Ratings

Drain Bias Voltage (Vdd1, Vdd2)	+6V
RF Input Power (RFIN) (Vdd = +5 Vdc)	+10 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 9.68 mW/°C above 85 °C)	0.63 W
Thermal Resistance (channel to ground paddle)	103.4 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vdd (R_{bias} = 10K)

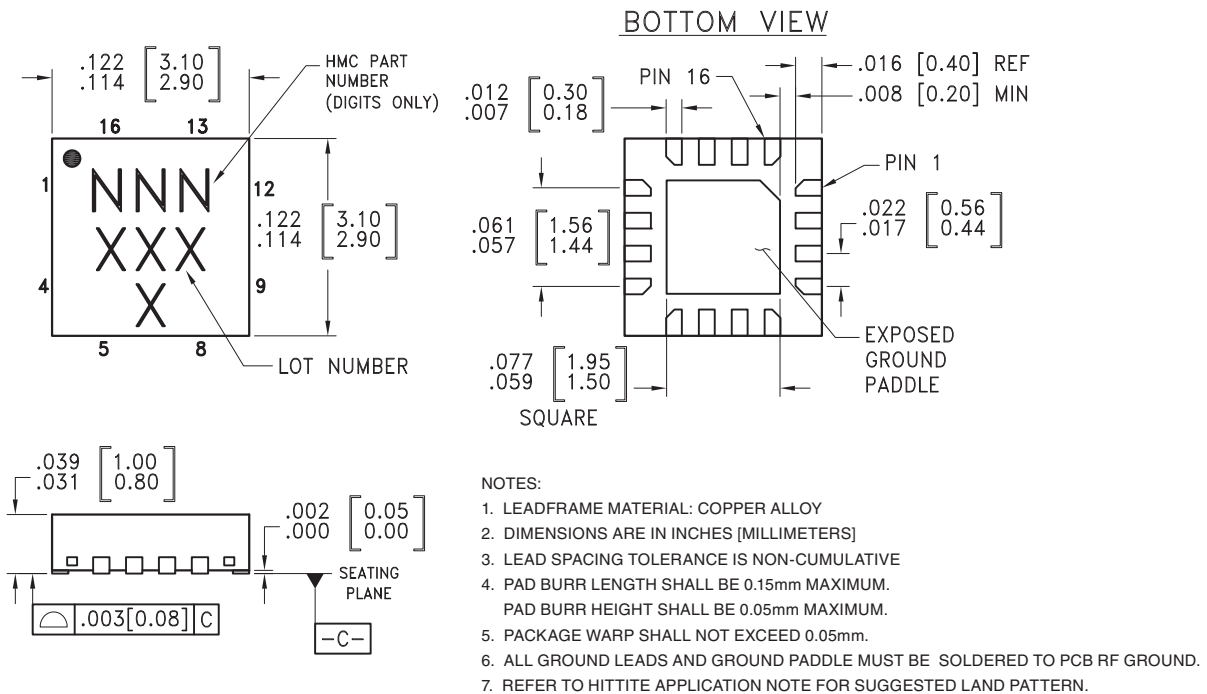
Vdd (Vdc)	Idd (mA)
2.7	35
3.0	47
3.3	58
4.5	101
5.0	117
5.5	133

Note: Amplifier will operate over full voltage ranges shown above.



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC618LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	618 XXXX
HMC618LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	618 XXXX

[1] Max peak reflow temperature of 235 °C

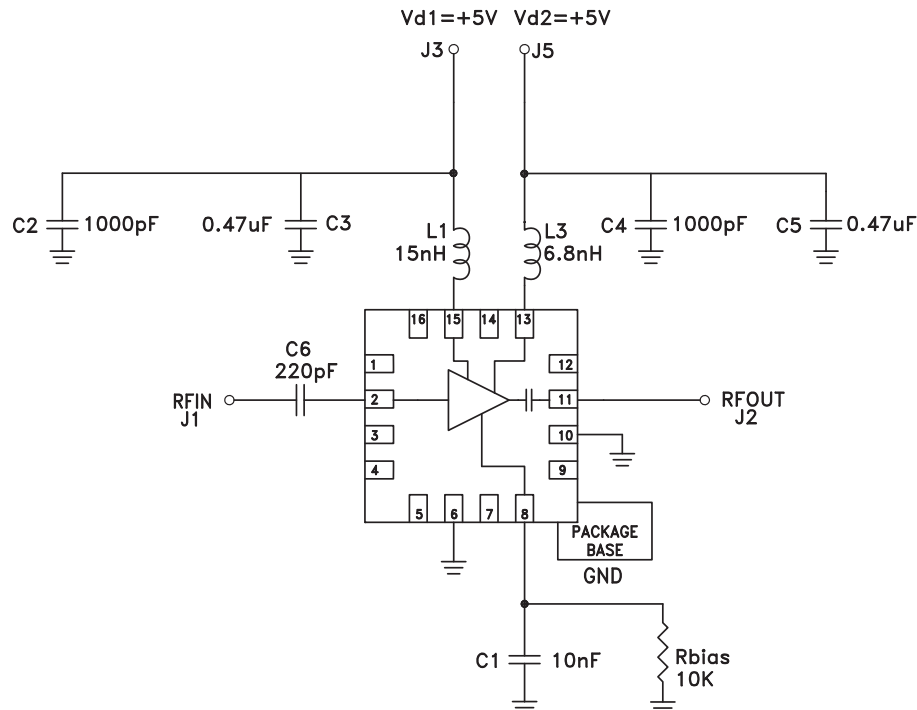
[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

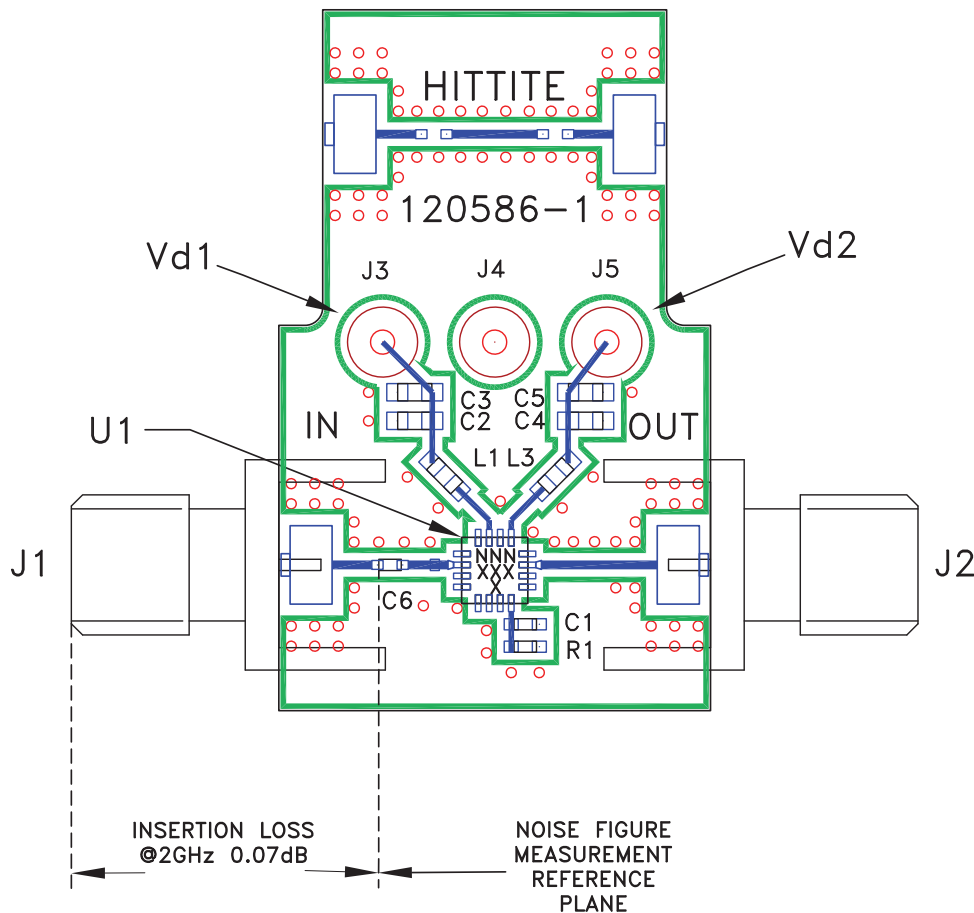
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3 - 5, 7, 9, 12, 14, 16	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
2	RFIN	This pin is DC coupled and matched to 50 Ohms.	
6, 10	GND	This pin and ground paddle must be connected to RC/DC ground.	
8	RES	This pin is used to set the DC current of the amplifier by selection of the external bias resistor. See application circuit.	
11	RFOUT	This pin is matched to 50 Ohms.	
13, 15	Vdd2, Vdd1	Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1000pF, and 2.2 μF are required.	

Application Circuit



Evaluation PCB



List of Material for Evaluation PCB 117905 [1]

Item	Description
J1, J2	PCB Mount SMA RF Connector
J3 - J5	DC Pin
C2, C4	1000 pF Capacitor, 0603 pkg.
C3, C5	0.47 μF Capacitor, Tantalum
L1	15nH, Inductor, 0603 pkg
L3	6.8nH, Inductor, 0603 pkg
C6	220pF Capacitor, 0402 pkg
C1	10nF Capacitor, 0402 pkg
R1	10k Ohm resistor, 0402 pkg
U1	HMC618LP3(E) Amplifier
PCB [2]	120586 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350.

The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.